IN THE CLAIMS

Please amend the claims as follows:

Claims 1-17 (Canceled).

Claim 18 (Previously Presented): A semiconductor device comprising:

a semiconductor substrate;

a gate oxide film formed on an element forming region of the semiconductor substrate;

a shallow trench insulation film formed in an element isolation region of the semiconductor substrate; and

a gate electrode film formed on the gate oxide film;

wherein the shallow trench insulation film has an upper surface positioned at a height between an upper surface and lower surface of the gate electrode film, and the shallow trench isolation film and the gate oxide film are doped with boron.

Claim 19 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

a gate insulation film formed on an element forming region of the semiconductor substrate;

a channel region formed in the element forming region beneath the gate insulation film, the channel region being doped with impurities of a predetermined conductivity type;

a gate electrode formed on the gate insulation film, the gate electrode including a first conductive film formed on the gate insulation film and a second conductive film formed on the first conductive film; and

a shallow trench isolation film formed in an element isolation region of the semiconductor substrate;

wherein the shallow trench isolation film, the gate insulation film and the first conductive film are doped with the same impurities as those doped in the channel region,

wherein the impurities include ~~are~~ boron.

Claim 20 (Previously Presented): A semiconductor device according to claim 19, wherein the shallow trench isolation film has an upper surface positioned at a height between an upper surface and lower surface of the gate electrode.

Claim 21 (Canceled).

Claim 22 (Previously Presented): A semiconductor device according to claim 19, wherein the impurities doped in the channel region, the gate insulation film and the first conductive film include phosphorus.

Claim 23 (Previously Presented): A semiconductor device according to claim 19, wherein the impurities doped in the channel region, the gate insulation film and the first conductive film have an impurity concentration peak in the semiconductor substrate at a predetermined depth from a surface of the semiconductor substrate.

Claim 24 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate including a first conductivity type transistor forming area and a second conductivity type transistor forming area;

a first gate insulation film formed on the first conductivity type transistor forming area;

a second gate insulation film formed on the second conductivity type transistor forming area;

shallow trench isolation films formed in the first and second conductivity type transistor forming areas;

a channel region formed in each of the first and second conductive type transistor forming areas beneath the first and second gate insulation films, the channel region being doped with impurities of a predetermined conductivity type; and

gate electrodes formed on the first and second gate insulation films, respectively, at least one of the gate electrodes including a first conductive film formed on the first or second gate insulation film and a second conductive film formed on the first conductive film;

wherein at least the shallow trench isolation films, the first gate insulation film and the first conductive film are doped with the same impurities as those doped in the channel region,

wherein the impurities include ~~are~~ boron.

Claim 25 (Previously Presented): A semiconductor device according to claim 24, wherein each of the shallow trench isolation films has an upper surface positioned at a height between an upper surface and lower surface of each of the gate electrodes.

Claim 26 (Canceled).

Claim 27 (Previously Presented): A semiconductor device according to claim 24, wherein the impurities doped in the channel region, at least the first gate insulation film and the first conductive film include phosphorus.

Claim 28 (Previously Presented): A semiconductor device according to claim 24, wherein the impurities doped in the channel region, at least the first gate insulation film and the first conductive film have an impurity concentration peak in the semiconductor substrate at a predetermined depth from a surface of the semiconductor substrate.

Claim 29 (Previously Presented): A semiconductor device according to claim 24, wherein a first transistor formed in the first transistor forming area has a first threshold value and a second transistor formed in the second transistor forming area has a second threshold value.

Claim 30 (Previously Presented): A semiconductor device according to claim 24, wherein the first gate insulation film has a breakdown voltage higher than that of the second gate insulation film.

Claim 31 (Previously Presented): A semiconductor device according to claim 30, wherein the first and second gate insulation films are formed of first and second oxide films, the first oxide film having a thickness larger than that of the second oxide film.

Claim 32 (Previously Presented): A semiconductor device according to claim 24, wherein the first conductive film is a floating gate electrode in a non-volatile memory transistor.